H2020 EPIC Project: Next-Generation Channel Coding Towards Terabit/s Wireless Communications

The EPIC project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 760150.

Onur SAHIN, InterDigital Europe

7 March, 2019

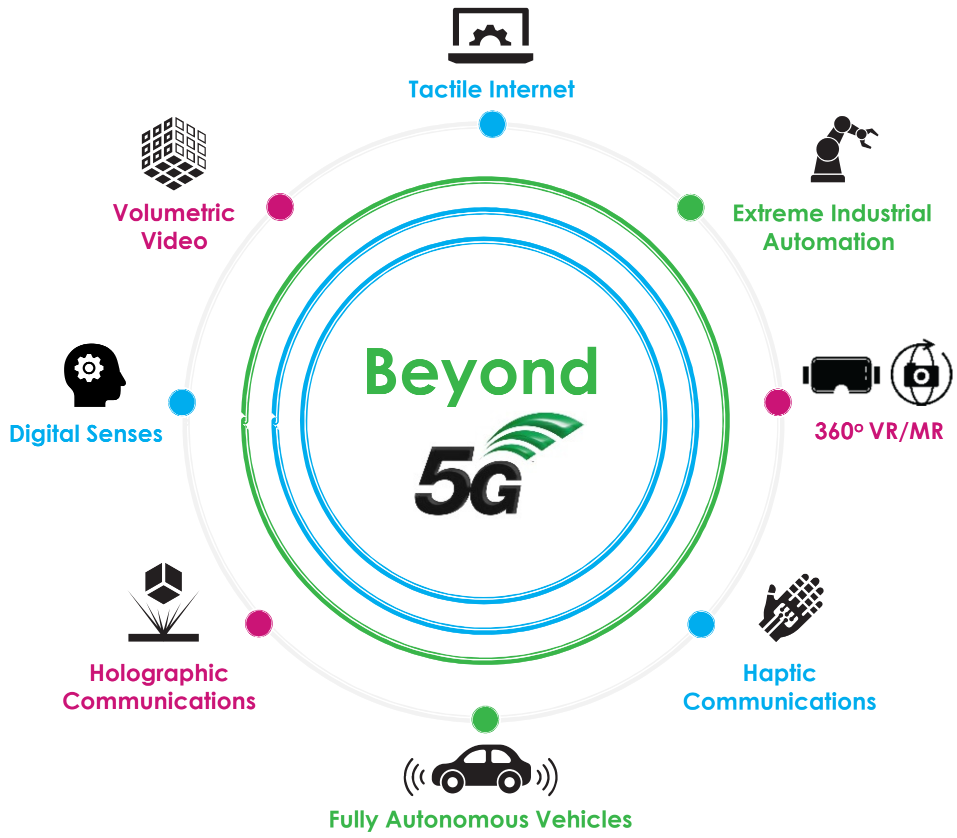
Topics Driving Beyond 5G: Immersive Applications & Services

Pervasive and truly immersive applications drive stringent requirements

Captivating virtual-meets-physical experiences: Unparalleled user-experiences drive need for ***multi-terabit/sec data rates, with sub-ms latencies***

Guaranteed high-precision services: Motion control with fast response demands **precise latencies as low as 10's of µsec**

Rearchitecting the digital world for full human-sense perception: Enabling digital senses requires **extreme low-latency, high availability and reliability**



What is EPIC? Exceeding 100 Gb/s Barrier in Wireless Communications

- EPIC project designs and implements next generation **FEC technology** (and relevant modulation modules) for a number of 5G and beyond (B5G) use cases, **primarily within ultra-high speed (>100Gbps) wireless systems (THz)**.
- 3-year (Sept 2017-Sept 2020) project is executed by 8 partners with in-depth expertise in coding theory&algorithm development, FEC implementation, and system-level design.

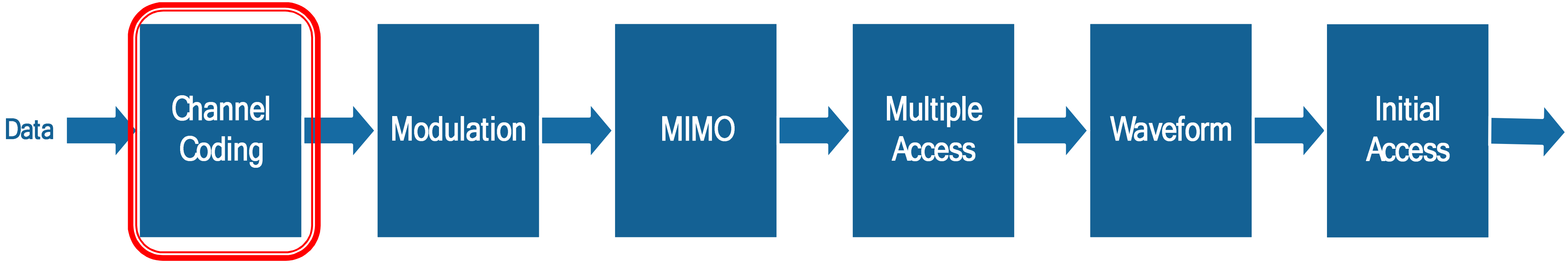


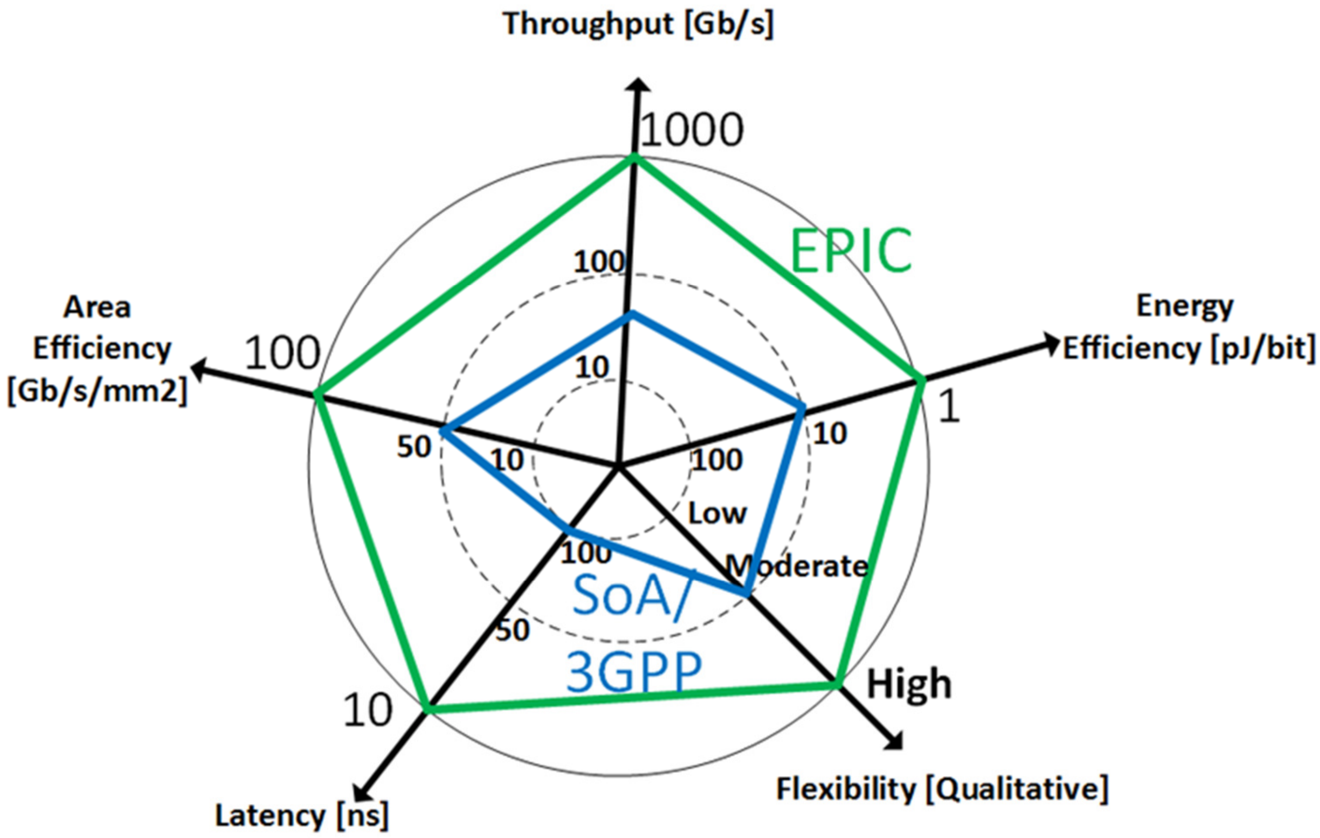
Fig: Abstracted link-level chain

Challenges Towards practical Tbps and FEC in B5G!

- FEC constitutes the most complex and computationally intense component in the baseband chain.
  - **Choke point for practical Tbps wireless technology with low-latency and high reliability.**
- 3G→4G→5G baseband and FEC implementations have enjoyed silicon scaling, a.k.a Moore's Law; 180nm→14nm/7nm
  - Higher transistor density, lower power consumption, lower power consumption.
- Impact of Moore's Law Slow-down:
  - **Power density** will emerge as a binding constraint
  - **Energy efficiency** will be critical
  - **The clock frequency** feasible value of 1 GHz
  - First profound impacts in 7nm/4nm and Beyond 5G

Practical B5G Tbps FEC KPI bounds	
Chip area limit	10 mm^2
Area efficiency limit	100 Gb/s/ mm^2
Energy efficiency limit	~1 pJ/bit
Power density limit	0.1 W/ mm^2

Channel Coding SoA vs EPIC Goals

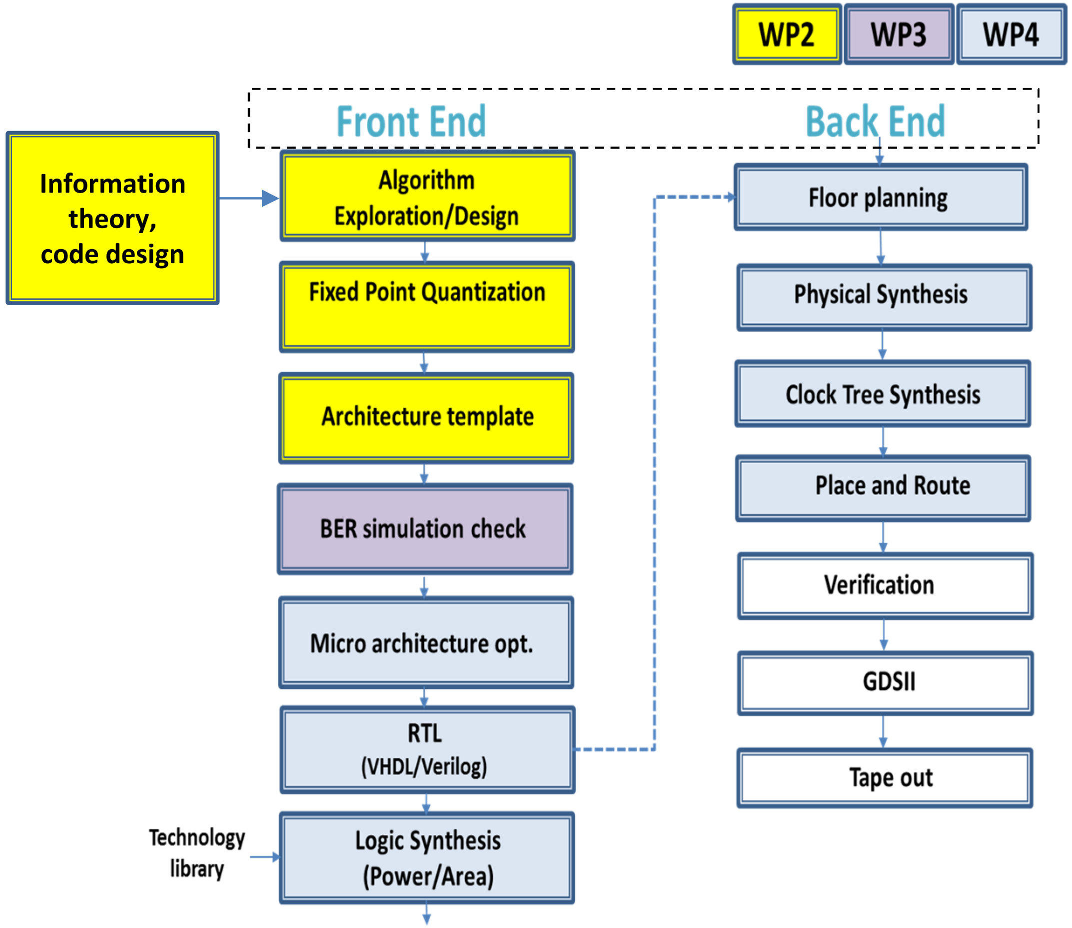


EPIC Methodology:
A powerful methodology that jointly develops encoder/decoder algorithms and architecture. The key enabler for the success of LDPC in the last 10 years. Same will be done for the new codes, inc. Polar.

3GPP (5G) figures:
Intel, "Comparison of channel coding schemes for NR", 3GPP Meeting #86, R1-166557,
Nokia, Alcatel-Lucent Shanghai Bell, Verizon Wireless, Xilinx "Implementation aspects of eMBB coding schemes", R1-167272

EPIC Innovation, Design, and Implementation Areas

- Implementation-aware FEC Algorithms:
  - Novel codes and decoding algorithms
  - Polar Codes, LDPC, Turbo Codes
- FEC Architectures:
  - Optimized encoder and decoder microelectronic architectures
  - Highly parallel and deep pipelined
- ASIC implementation (front-end and back-end):
  - Implementation of selected codes in deeply-scaled CMOS
  - Target technology node: 7nm CMOS



EPIC Studies and Outcomes

B5G use-cases and system-level&FEC requirements

- Thorough exploration of potential wireless ultra-high throughput use-cases for B5G.
  - System requirements and KPIs (bit and frame error rate, throughput, latency, power, cost, flexibility)
  - FEC level-KPIs utilizing system requirements (bit and frame error rate, throughput, latency, energy efficiency, area efficiency, and power density)

	BER	Flexibility	Latency	Throughput [Gbps]
Virtual reality	10^-6	high	0.5ms	500,00
Data kiosk	10^-12	low	0.5ms	1000,00
Backhaul	10^-8	medium	100ns	250,00
Intra-device com.	10^-12	low	100ns	500,00
Fronthaul	10^-12	medium	25ns	1000,00
Data center	10^-12 ~ 10^-15	medium	100ns	1000,00
Hybrid wireless fiber	10^-12	medium	200ns	1000,00
High speed satellite	10^-10	medium	max ~10ms	100-1000

Where We are Today in EPIC Project towards Tb/s

OVERVIEW ON IMPLEMENTATION PROPERTIES

Code	Decoding algorithms	Parallel vs. serial	Locality	Compute kernels	Transfers vs. compute
Turbo code	MAP	serial/iterative	low (interleaver)	Add-Compare-select	compute dominated
LDPC code	Belief propagation	parallel/iterative	low (Tanner graph)	Min-Sum/add	transfer dominated
Polar code	Successive cancelation/List	serial	high	Min-Sum/add/sorting	balanced

28nm low V_t FDSOI Technology, worst case PVT, after Place & Route

Code	Blocksize [bit]	Code rate	Frequency [MHz]	Throughput [Gbit/s]	Area [mm^2]	Power [mW]	Area efficiency [Gbit/s/mm^2]	Energy efficiency [pJ/bit]
Turbo code (4 iter)	128	1/3	800	102	23.6	-	4.34	-
LDPC code (9 iter)	672	13/16	400	268	2.8	1500	95.7	5.6
LDPC code (4 iter)	672	13/16	400	268	1.3	700	215	2.5
Polar code	1024	1/2	746	764	2.95	3300	259	4.4

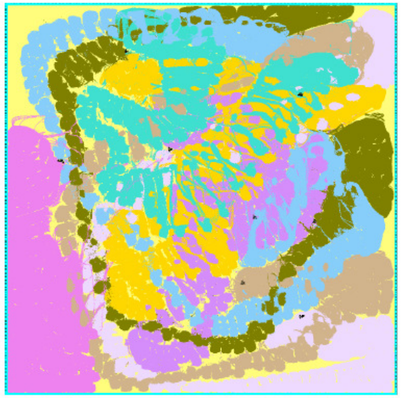


Fig. 1. 102 Gbit/s Turbo code decoder, area 23.61 mm^2

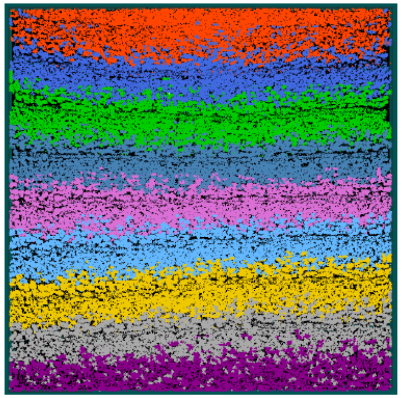


Fig. 2. 268 Gbit/s LDPC code decoder, area 2.8 mm^2

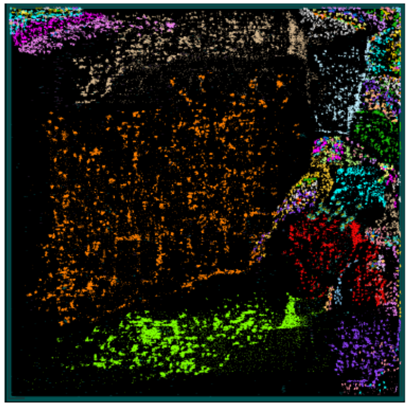


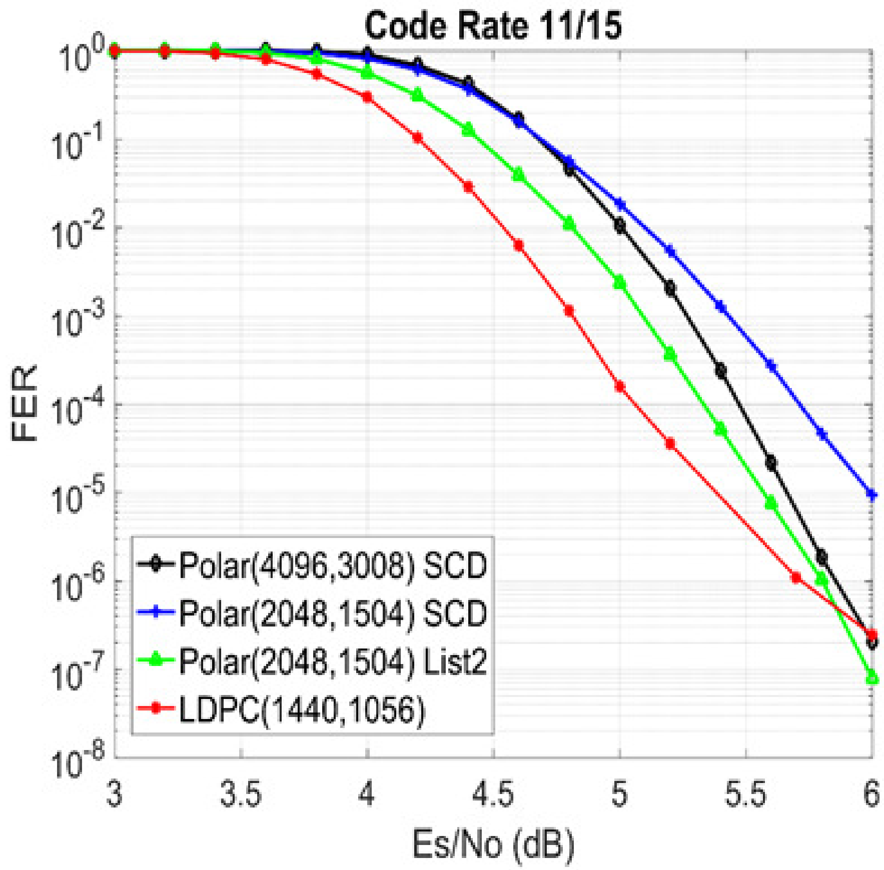
Fig. 3. 764 Gbit/s Polar code decoder, area 2.95 mm^2

Communications Performance Comparison: LDPC vs Polar Codes

- EPIC FEC classes evaluated :
  - **IEEE 802.15.3d LDPC**: Length-1440, Rate=11/15.
  - **Polar codes**: Length(L) = 2048, 4096, Rate=11/15. List-size=1,2 (CRC=8bits). Density (D) evolution based code design.

Observation:

- Polar codes (L=4096, List-size=1 and Polar code L=2048, List-size=2) are able to compete with LDPC codes at SNRs greater than 6dB.
- LDPC code experiences degraded performance at high SNRs (>6dB), a critical range for THz use-cases.



- Modulation: QPSK
- AWGN channel (BH/FH use-case in 802.15.3d study)

Conclusion

- Significant progress made in 100 Gb/s→1 Tb/s LDPC and Polar code design and implementations.
- Challenges remain for a completely practical B5G Tb/s FEC solution, but target reachable.
- Innovations on both algorithmic and implementation fronts.
- EPIC project is dedicated to solve the Tbps FEC bottleneck.
- Project progress and reports are available at: https://epic-h2020.eu/.

General Project Information

- Project reference: **760150**
- Project start: **1st September 2017**
- Duration: **3 years**
- Total costs/EC contribution: **EUR 2.966.268,75**
- **Eight partners** from **seven** different **European countries:**
  - Creonic Gmbh , Ericsson AB, IMEC, Institut Mines-Telecom, InterDigital Europe, Polaran, Technikon, Technische Universitaet Kaiserslautern
- **Mission:** EPIC aims to develop a new generation of Forward-Error-Correction (FEC) codes in a manner that will serve as a fundamental enabler of practicable beyond 5G wireless Tb/s solutions and also to develop and utilize a disruptive FEC design framework allowing to advance state-of-the-art FEC schemes.
- Website: www.epic-h2020.eu
- Twitter: Epic760150; Linkedin: https://www.linkedin.com/in/epic-project-184362150

Partners:

TECHNIKON	Technikon Forschungs- und Planungsgesellschaft mbH (Coordinator) Villach, Austria
INTERDIGITAL EUROPE	InterDigital Europe Ltd. London, United Kingdom
imec	Interuniversitair Micro-Electronica Centrum (imec) Leuven, Belgium
POLARAN	Polaran Ltd. Ankara, Turkey
TECHNISCHE UNIVERSITÄT KAISERSLAUTERN	Technische Universität Kaiserslautern (Technical Lead) Kaiserslautern, Germany
ERICSSON	Ericsson AB Stockholm, Sweden
IMT Atlantique Bretagne-Pays de la Loire École Mines-Télécom	Institut Mines-Télécom, IMT Atlantique Brest, France
CREONIC ip cores & system solutions	Creonic GMBH Kaiserslautern, Germany

EPIC Grant Agreement No. 760150

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Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding