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SCALABLE mmW ARCHITECTURE AND IMPLEMENTATION TOWARDS THZ SOLUTIONS

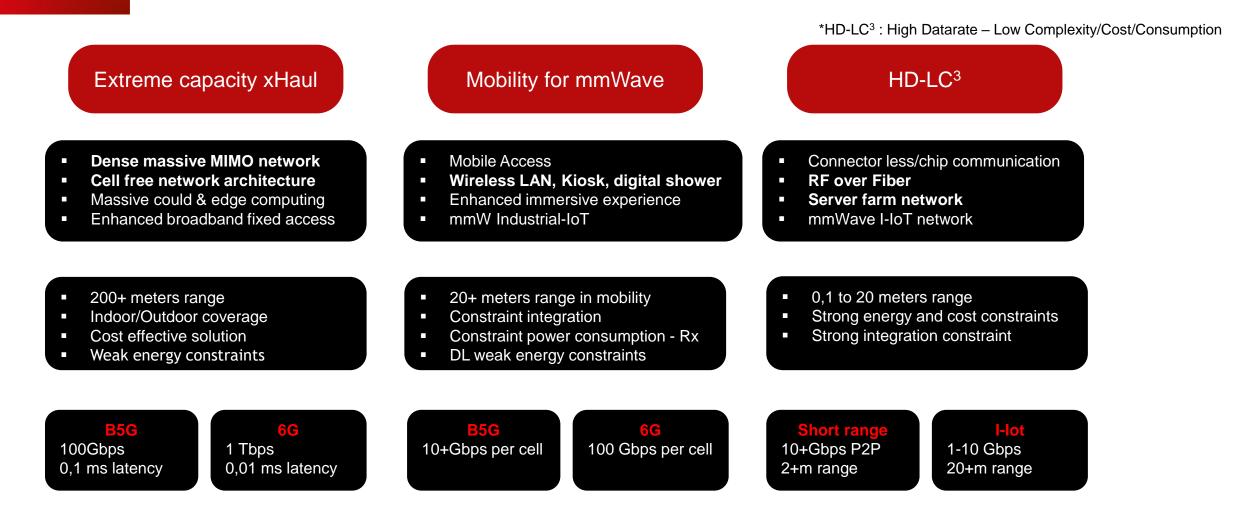
3TTCW, 12th March 2021 Eric Mercier

- 5G current deployment
 - NR FR1 : below 6 GHz frequency bands , mainly **3.5 GHz** today
 - NR FR2 : mmW frequency bands, 26 GHz 29 GHz / 38 GHz 40 GHz
- Addressed challenges
 - FR1: 100 MHz bandwidth up to 400 MHz aggregated
 - FR2: 400 MHz bandwidth up to 800 MHz aggregated
- Beyond current 5G ... much larger bandwidth
 - New FR3 : V-band (60 GHz), W-band (above 91 GHz)
 - New FR4 : D-band (120 GHz to 170 GHz)
 - And forthcoming **285 GHz 300 GHz** trials
- Much higher throughputs : target above 100 Gbps

... and mandatory consideration of a power hungry wideband process

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USE CASE FOR mmW / SUB-THz AT A GLANCE



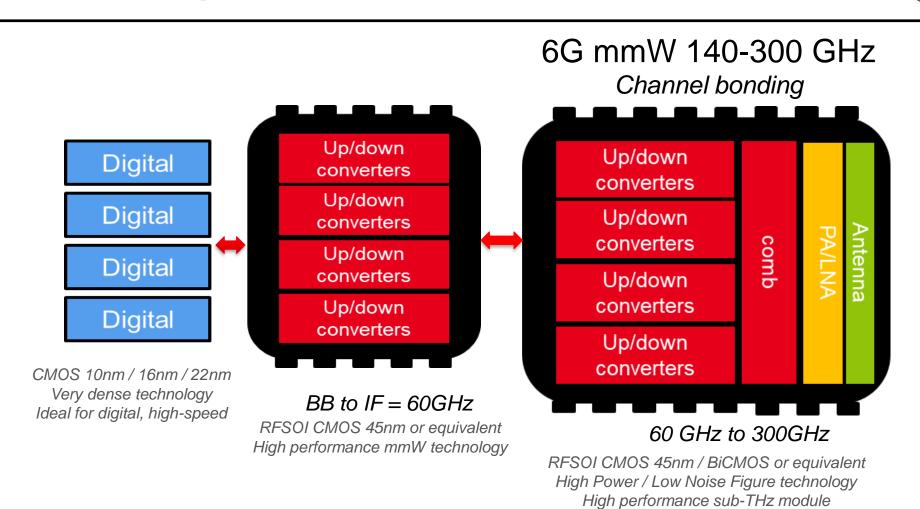
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A SCALABLE APPROACH ENVISIONING UPGRADES

From D-BB to 60 GHz, up to 140 GHz even 300 GHz

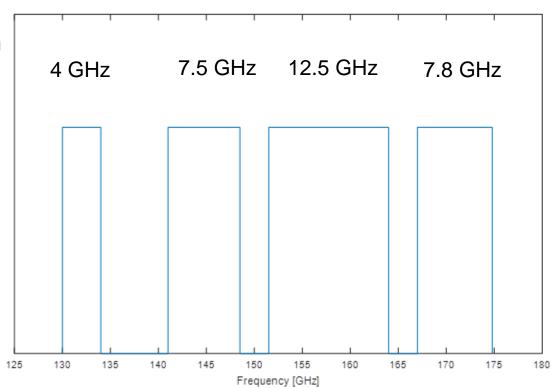




USING THE D-BAND TO ITS FULL CAPACITY

- Frequency plan in a very wideband domain
 - Multiple sub-bands & channels to be considered
 - Classical approach for transceiver would :
 - Use multiple Local Oscillator
 - Consider very wideband Rx & Tx chain

... but a huge potential in D-Band

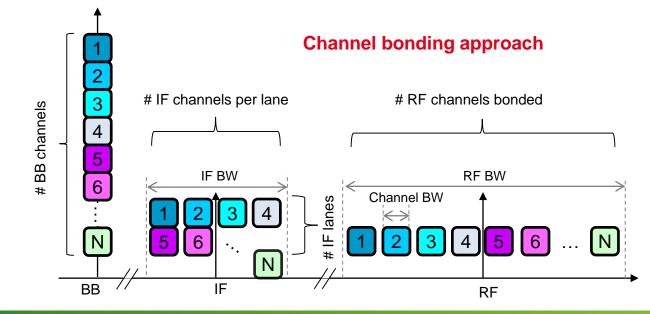




CHANNEL BONDING TRANSCEIVER ARCHITECTURE

Dedicated architecture making use of efficient frequency plan

- 4 Lanes with 4 sub-channels
 - 16 x channels are considered at BB level
 - 4 x IF at 60 GHz build one lane
 - 4 x lanes are recombined at D-band level
 - Passive recombination at PA level





TRANSCEIVER IMPLEMENTATION

Dedicated architecture making use of efficient frequency plan

- Transceiver SoC for 100 Gbps Wireless point-to-point links
 - A few meters of distance range
 - Output power is not

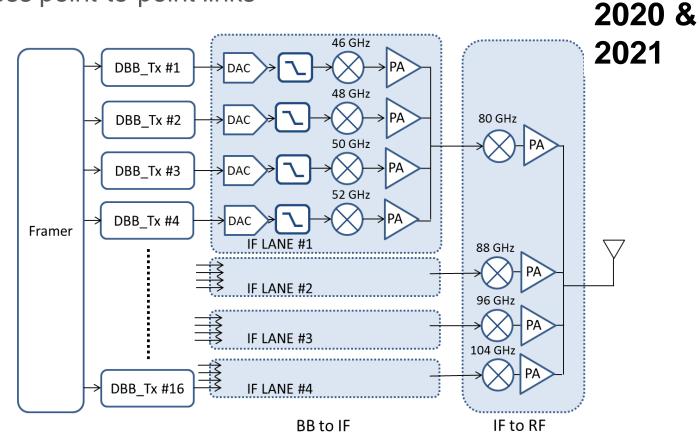
the key target performance

- Passive recombination at PA level
 - Best way for efficiency on Tx
- 4 upconverters / downconverters

for each lanes

for each mmW path

Mandatory need for low phase noise



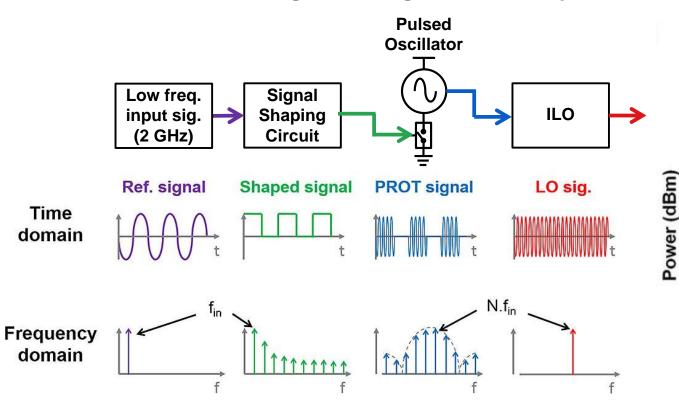
ONFIDENTIAL Architecture eventually avoiding complex, power consuming ADC & DAC



LOW PHASE NOISE mmW FREQUENCY SYNTHESIS

Multi-LO frequency generator

60 GHz / WiGig band LO generator example

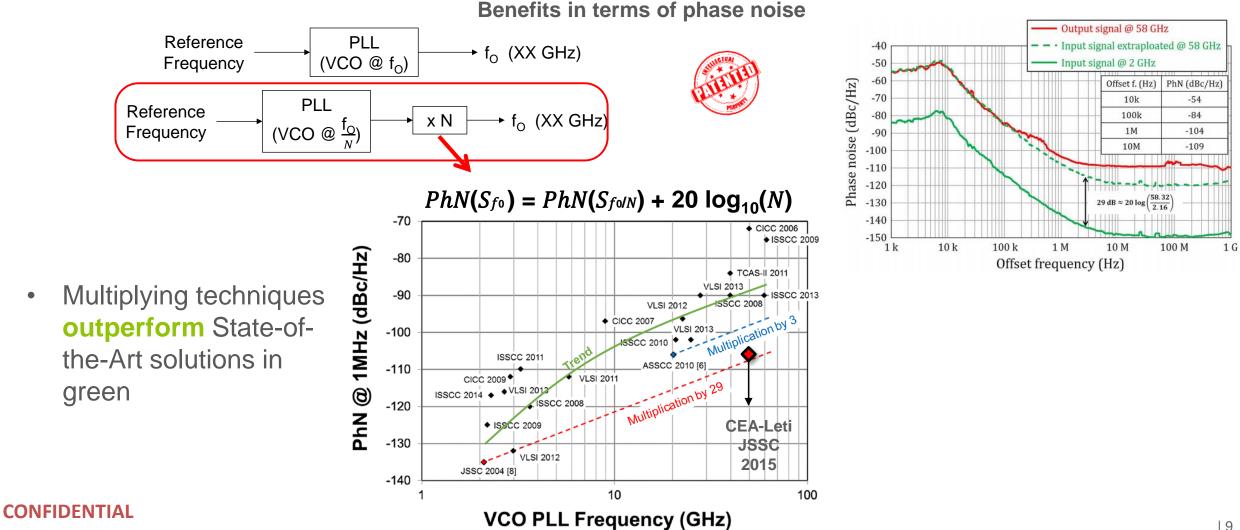


Alexandre Siligaris, José Luis Gonzalez-Jimenez, & altri "A Multichannel Programmable High Order Frequency Multiplier for Channel Bonding and Full Duplex Transceivers at 60 GHz Band," RFIC 2020.

UNDRIES Pulsed osc. output signal **Channel 1 selected** -20 58.32 GHz -32 dB -40 -60 -80 **Channel 2 selected** -20 RBW: 1 MHz 60.48 GHz VBW: 10 MHz -40 31 dB Sw.T: 60 msec -60 -80 Channel 3 selected 16 GHz -20 62.64 GHz--40 31 dB -60 -80 53 55 57 63 65 67 59 61 Frequency (GHz)



Multi-LO frequency generator

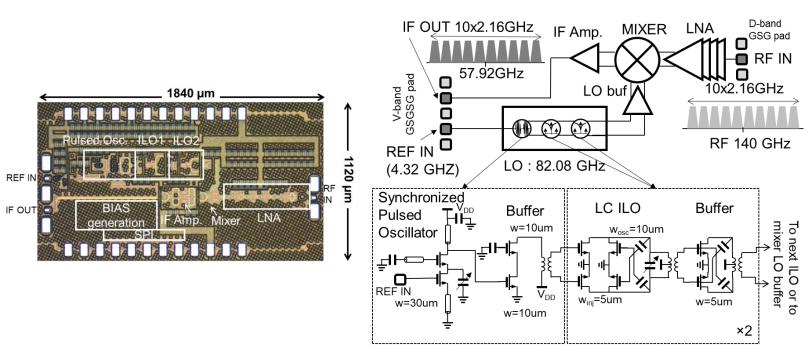




HIGH-SPEED WIRELESS COMMUNICATIONS TRANSCEIVER - TRANSMITTER

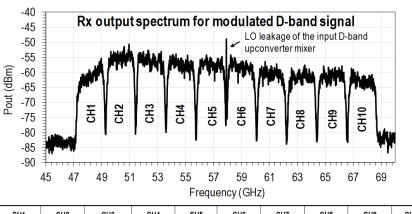
Receiver - 108 Gbps / 64QAM / 10 channels

- Transposition of D-band to V-band Receiver
- 10 sub-channels are received simultaneously









CH1	CH2	СНЗ	CH4	CH5	CH6	CH7	CH8	СН9	CH10
130.28GHz	132.44GHz	134.60GHz	136.76GHz	138.92GHz	141.08GHz	143.24GHz	145.40GHz	147.56GHz	149.72GHz
1.8Gbauds									
****		* * * *					* * * *		* * * * * * * * * * * *
EVM=6.8%	EVM=6.0%	EVM=5.4%	EVM=5.4%	EVM=5.4%	EVM=5.5%	EVM=6.2%	EVM=6.5%	EVM=6.3%	EVM=6.6%
7.2Gb/s									
EVM=6.7%	EVM=6.2%	EVM=5.1%	EVM=5.4%	EVM=5.4%	EVM=5.3%	EVM=5.7%	EVM=5.7%	EVM=5.5%	EVM=6.6%
10.8Gb/s									

Alexandre Siligaris, José Luis Gonzalez-Jimenez, & altri " A 125.5-157 GHz 8 dB NF and 16 dB of Gain D-band Low Noise Amplifier in CMOS SOI 45 nm," IMS 2020



IF input splitter

SPI digital interface

2100 µm

and matching

LOLB

Z

1420

BIAS

DAC

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HIGH-SPEED WIRELESS COMMUNICATIONS TRANSCEIVER - TRANSMITTER

This work's IC 4x2.16GHz

IEcu

IF_C

IF_{CH2}

62.28GHz

LOUB 91.665GHz

IF combiner

LO_{LB} 82.935GHz

4x2.16GHz

62.28GHz

D-band

combiner

🗖 RF OUT

I R

8x2.16GHz

149.58GHz

UB

Transmitter - 84.48 Gbps / 64QAM / 8 channels

- Transposition of V-band to D-band Transmitter

8

8x2.16GHz BB channels

Power

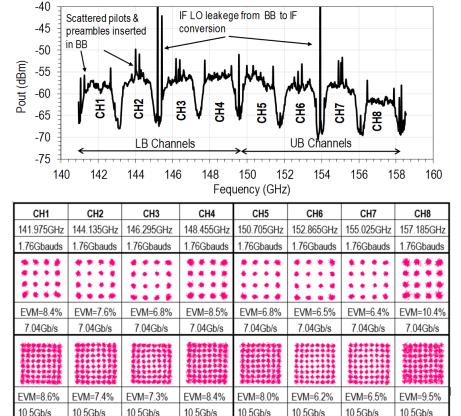
PA LB

- 2 x Lanes of 4 x sub-channels have been implemented



Channel 1.2

LO_{IFCH1}





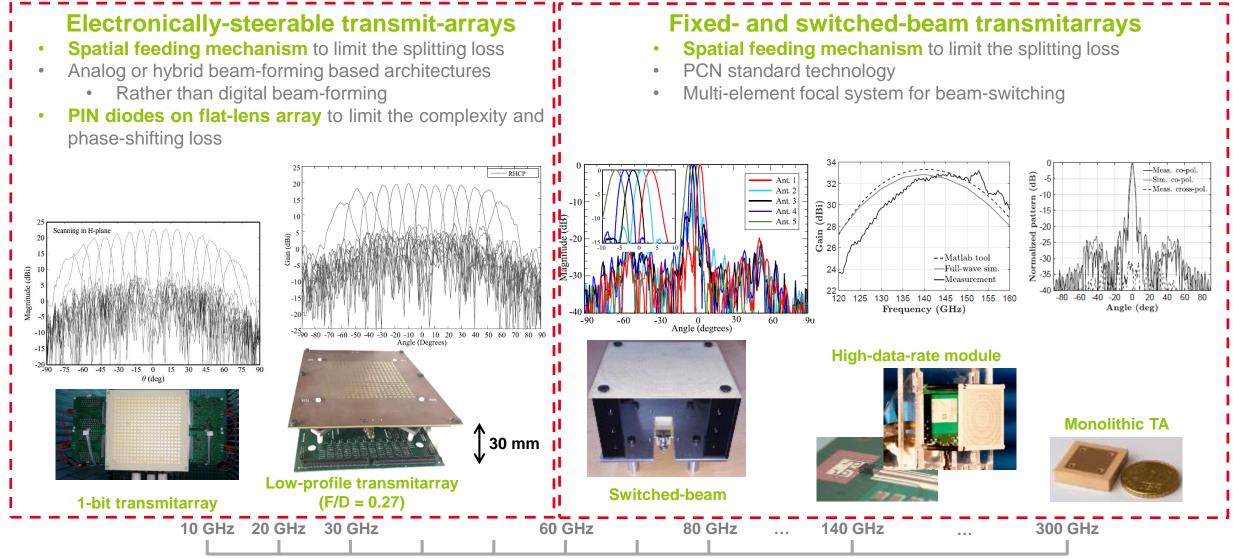




CONCLUSIONS ON THE D-BAND USE

- Transceiver implementation
 - Demonstration is done that a smart implementation can address 100 Gbps
 - Soon, publications about a full 16-channel of BW=2.16 GHz
 - High potential of ILO-based Frequency generation for low Phase Noise
 - But still limited range as CMOS does not produce high power/low Noise Figure at 140 GHz
 - Nevertheless, **OK for HD-LC³** (High Datarate Low Complexity/Cost/Consumption)
- Next steps to improve performance / distance range
 - Scalable approach :
 - keep a V-band transceiver, processing sub-channels in different lanes, onto CMOS technology
 - Address V-band to D-band with a different technology, higher-end
 - Option 1 :
 - Full-transceiver from D-BB to D-Band in CMOS
 - Front-End Module using high-end technology to improve output power/NF
 - Option 2 :
 - Consider high directivity gain for the antenna to compensate for CMOS limitations

ELECTRONICALLY-STEERABLE TRANSMIT-ARRAY



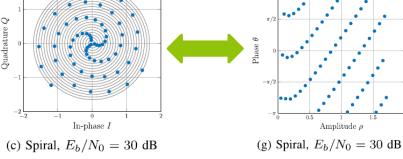
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PHY OPTIMIZATION FOR THROUGHPUT IMPROVEMENT

- Increasing frequencies means increased Phase Noise
 - Phase Noise improvements lead to higher power consumption
 - Consider modulation scheme for more robustness
- Optimized Symbol Error Rate
 - Rather than BER, symbols are KPI
 - Find a way to maximize the minimum distance Symbol Error Ratu
 - Polar-QAM with 2 parameters :
 - M : modulation order & Γ : number of circles

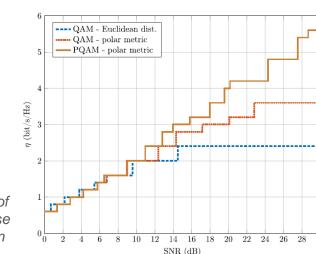


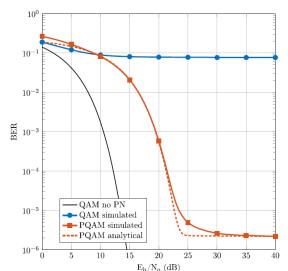
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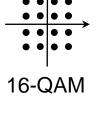
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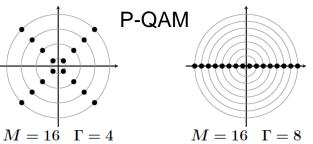
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Simon Bicaïs & Jean-Baptiste Doré, "Design of Digital Communications for Strong Phase Noise Channels", IEEE Open Journal on Vehicular Technology, Vol. 1 2020



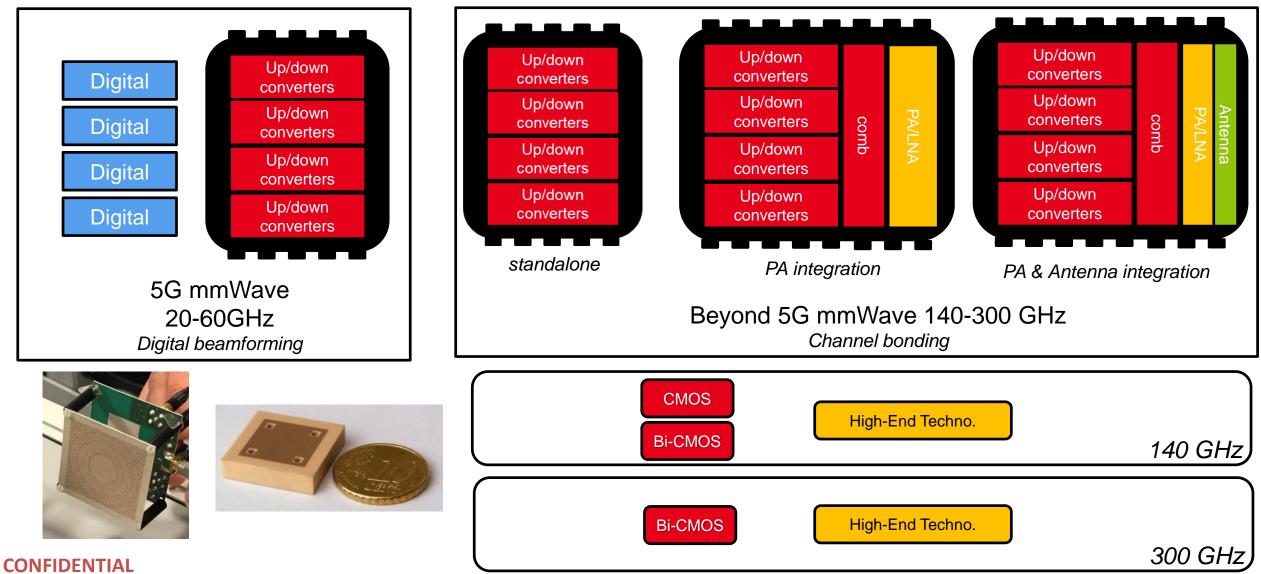




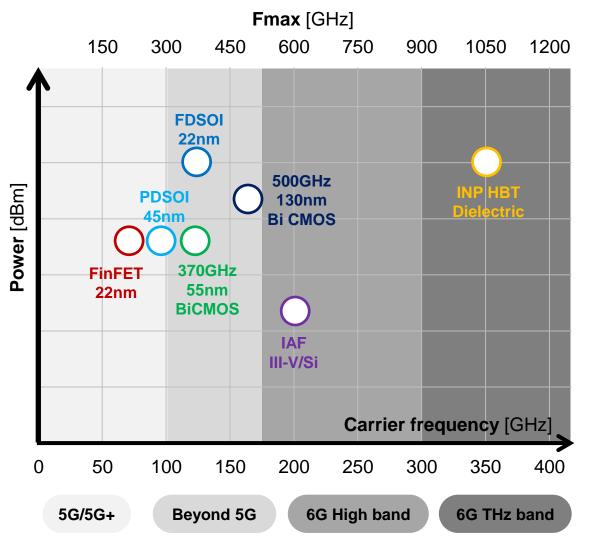


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INTEGRATION PERSPECTIVES

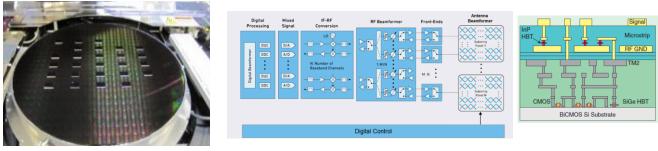


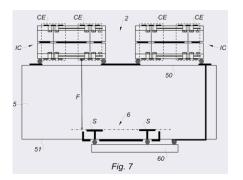
CONCLUSION ON INTEGRATION & TECHNOLOGY PERSPECTIVES

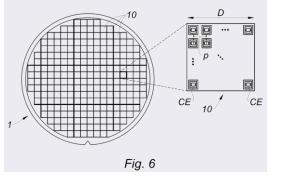


- **RF bands : room from 100 GHz to 300 GHz**
- 100Gbps full-transceivers made possible
- RF, mmW, Antenna co-design
- Next CMOS frontiers :
 - New transistors, new materials

Hybridation

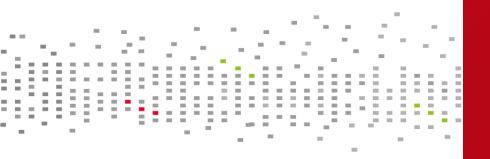






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